**Swift GTi 64xxx UPP initialisation**

UDR is a 2 byte register with addresses starting at 40h (1040h)

FNR = Function number 0 to 14

to program function table set FNR=n then write to 023->029

23 = Command register

24 = Register Assignment register A - UDR register to be used as a counter/timer/Shifter

25 = Register Assignment register B - UDR register to be used as a capture/compare/data(shift)

26 = IO Assignment Register A - clock input pin number and edge direction for RASRA

27 = IO Assignment Register B - pulse input pin number and edge direction for RASRB

28 = IO Assignment Register C - pulse output pin number

29 = IO Assignment Register D - pulse input pin - gate signal or trigger enable

MFNR = 0 = 16 functions

010 = UCER2 -> contact enable register

011 = UCER1 1=pulse I/O, 0=port I/O

ISR1-3 set on an interrupt on INT0 (U0-U15) or INT1 (U16-23) - upper 4-bits rising edge/lower 4-bits falling edge

IER1-3 enables interrupts

IRQR1-IRQR3 - logical AND of ISR and IER

ISCR - 0 = clear interrupt, 1= hold interrupt

UPP Init:

ROM:DD34 fcb 1,$61,$E0,$EC,$FF,$B0,$EC,$FF; 0

ROM:DD34 fcb 2,$B0,$E1,$ED,$FF,$CA,$E2,$F4; 8

ROM:DD34 fcb 3,$70,$E2,$EE,$FF,$C2,$E0,$FF; 16

ROM:DD34 fcb 4,$10,$E3,$EF,$FF,$CA,$E3,$FF; 24

ROM:DD34 fcb 6,$50,$E4,$F0,$FF,$FF,$E4,$FF; 32

ROM:DD34 fcb 7,$61,$E5,$F1,$FF,$C4,$EE,$FF; 40

ROM:DD34 fcb 8,$50,$E6,$F2,$FF,$FF,$E5,$FF; 48

ROM:DD34 fcb 9,$60,$E7,$F3,$FF,$C5,$EF,$FF; 56

ROM:DD34 fcb $B,$50,$E8,$F4,$FF,$FF,$E1,$FF; 64

ROM:DD34 fcb $C,$48,$E9,$F5,$EB,$FF,$FF,$FF; 72

ROM:DD34 fcb $D,$48,$EA,$F6,$C9,$FF,$FF,$FF; 80

ROM:DD34 fcb $E,$48,$EB,$F7,$C8,$FF,$FF,$FF; 88

ROM:DD34 fcb $10,$FF,$FF,$FF,$FF,$FF,$FF,$FF; 96

ROM:DD34 fcb $11,$FF,$FF,$FF,$FF,$FF,$FF,$FF; 104

ROM:DD34 fcb $12,$FF,$FF,$FF,$FF,$FF,$FF,$FF; 112

ROM:DD34 fcb $13,$FF,$FF,$FF,$FF,$FF,$FF,$FF; 120

Functions 0,5,10 are not available to the user.

**UPP register settings:**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| FN | GTi | CMR | | RASRA | RASRB | IORA  (CLK) | IORB | IORC | IORRD |
| 0 |
| 1 | INJ | **61** | PWC | **E0** | **EC** | **FF** | **B0** | **EC** | **FF** |
| 2 | IGN | **B0** | CTO | **E1** | **ED** | **FF** | **CA** | **E2** | **F4** |
| 3 | IGN | **70** | OSC | **E2** | **EE** | **FF** | **C2** | **E0** | **FF** |
| 4 |  | **10** | INS | **E3** | **EF** | **FF** | **CA** | **E3** | **FF** |
| 5 |
| 6 |  | **50** | INC | **E4** | **F0** | **FF** | **FF** | **E4** | **FF** |
| 7 | ISC | **61** | PWC | **E5** | **F1** | **FF** | **C4** | **EE** | **FF** |
| 8 |  | **50** | INC | **E6** | **F2** | **FF** | **FF** | **E5** | **FF** |
| 9 |  | **60** | PWC | **E7** | **F3** | **FF** | **C5** | **EF** | **FF** |
| A |
| B |  | **50** | INC | **E8** | **F4** | **FF** | **FF** | **E1** | **FF** |
| C | VSS | **48** | FRC | **E9** | **F5** | **EB** | **FF** | **FF** | **FF** |
| D | IFS | **48** | FRC | **EA** | **F6** | **C9** | **FF** | **FF** | **FF** |
| E |  | **48** | FRC | **EB** | **F7** | **C8** | **FF** | **FF** | **FF** |
| F |
| 10 |  | **FF** | NOP |  |  |  |  |  |  |
| 11 |  | **FF** | NOP |  |  |  |  |  |  |
| 12 |  | **FF** | NOP |  |  |  |  |  |  |
| 13 |  | **FF** | NOP |  |  |  |  |  |  |

CMR is the command register

RASRA is the UDR functioning as a counter or timer register.

RASRB is the UDR functioning as a capture or compare register

IORA is the clock select register

IORB is the sampling or trigger or reset register

IORC is the pulse output pin select register

IORD is the pulse input pin select register

**Function 1 – Pulse Width Timer with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

61 = Pulse Width Timer, triggers on Rising Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

E0 = UDR0 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

EC: UDR12 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable increment on falling edge of signal U15

REDGA = 1, enable increment on rising edge of signal U15

CMD, bit3 =0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

B0: FEDGB = 0, disable trigger on falling edge

REDGB = 1, enable trigger on rising edge

SPN = 16, Trigger input pin = U16 = UIOR, bit0

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

EC: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LBNA = C, pulse output pin = U12 = P24 = pin 36

**IORD – I/O (Pulse I/P Pin) Assignment Register**

Not used in a PWC implementation.

**Function 2 – Combination Trigger One Shot Timer**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

B0 = Combination Trigger One Shot Timer, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

E1 = UDR1 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

ED: UDR13 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD C/T=0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

CA: FEDGB = 0, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

SPN = 10, Trigger input pin = U10 = P22 = pin 38

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

E2: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = 2, pulse output pin = U2 = P12 = pin 46

**IORD – I/O (Pulse I/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNB[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

F4: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNB = F, pulse input pin = U20 = UIOR, bit 4

**Function 3 –One Shot Timer with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

70 = One Shot Timer with compare, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

E2 = UDR2 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

EE: UDR14 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

C2: FEDGB = 0, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

SPN = 2, Trigger input pin = U2 = P12 = pin 46

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

E0: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = 0, pulse output pin = U0 = P10 = pin 48

**IORD – I/O (Pulse I/P Pin) Assignment Register**

Not used with OSC function

**Function 4 – Interval Timer with Sampling**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

10 = Interval Timer with sampling, internal clock, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

E3 = UDR3 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

EF: UDR15 is the capture register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

CA: FEDGB = 0, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

SPN = 10, sampling pin = U10 = P22 = pin 38

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

E3: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = 3, pulse output pin = U3 = P13 = pin 48

**IORD – I/O (Pulse I/P Pin) Assignment Register**

Not used for this function

**Function 5 is used internally by the UPP**

**Function 6 – Interval Timer with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

50 = Interval Timer with compare, internal clock, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

E4 = UDR4 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

F0: UDR16 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

FF - IORB is not used by this function

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

E4: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = 4, pulse output pin = U4 = P14 = pin 44

**IORD – I/O (Pulse I/P Pin) Assignment Register**

Not used for this function

**Function 7 – Pulse Width Timer with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

61 = Pulse Width Timer with sampling, internal clock, triggers on Rising Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

E5 = UDR5 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

F1: UDR17 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

C4: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

SPN = 4, pulse input pin = U14 = P24 = pin 36

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

EE: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = E, pulse output pin = U14 = P26 = pin 34

**IORD – I/O (Pulse I/P Pin) Assignment Register**

FF - Not used for this function

**Function 8 – Interval Timer (output) with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

50 = Interval Timer (output) with compare, internal clock, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

E6 = UDR6 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

F2: UDR18 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

FF: Not used for this function

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

E5: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = 5, pulse output pin = U5 = P15 = pin 43

**IORD – I/O (Pulse I/P Pin) Assignment Register**

FF - Not used for this function

**Function 9 – Pulse Width Timer with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

60 = Pulse Width Timer with compare, internal clock, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

E7 = UDR7 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

F3: UDR19 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

C5: FEDGB = 0, disable trigger on falling edge

REDGB = 1, enable trigger on rising edge

SPN = 5, Trigger input pin = U5 = P15 = pin 43

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

EF: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = F, pulse output pin = U15 = P27 = pin 33

**IORD – I/O (Pulse I/P Pin) Assignment Register**

Not used for this function

**Function 10 – Internal use**

**Function 11 – Interval Timer with Compare**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

50 = Interval Timer with compare, internal clock, triggers on Falling Edge

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

E8 = UDR8 is the timer for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

F4: UDR20 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CMD, bit3 = 0, internal clock

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

FF: Not used for this function

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

E1: FEDGB = 1, enable trigger on falling edge

REDGB = 1, enable trigger on rising edge

LPNA = 1, pulse output pin = U1 = P11 = pin 47

**IORD – I/O (Pulse I/P Pin) Assignment Register**

FF - Not used for this function

**Function 12 – Free Running Counter**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

48 = Free running counter, external clock

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

E9 = UDR9 is the counter for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

F2: This register is not used in this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |

EB: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CPN = B, U11, P23, pin 37

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

FF: Not used for this function

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: LPNA = 31, no output pin?

**IORD – I/O (Pulse I/P Pin) Assignment Register**

FF - Not used for this function

**Function 13 – Free Running Counter**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

48 = Free running counter, external clock

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

EA = UDR10 is the counter for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

F6: UDR22??

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

C9: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CPN = 9, U9, P21 pin 39

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: Not used for this function

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: LPNA = 31, no output pin?

**IORD – I/O (Pulse I/P Pin) Assignment Register**

FF - Not used for this function

**Function 14 – Free Running Counter**

**CMR – Command Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD[3-0] | | | | C/~T | 0 | 0 | H/~L |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

48 = Free running counter, external clock

**RASRA – UDR (Counter/Timer) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CTN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

EB = UDR11 is the counter for this function

**RASRB – UDR (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | -- | -- | CCN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

F7: UDR23 is the compare/reset register for this function

**IORA – I/O (Clock) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGA | REDGA | CPN[4-0] | | | | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

C8: FEDGA = 1, enable counting on falling edge of signal Up

REDGA = 1, enable counting on rising edge of signal Up

CPN = 8, U8, P20 pin 40

**IORB – I/O (Capture/Compare) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | SPN[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: Not used for this function

**IORC – I/O (Pulse O/P Pin) Assignment Register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -- | FEDGB | REDGB | LPNA[4-0] | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF: LPNA = 31, no output pin?

**IORD – I/O (Pulse I/P Pin) Assignment Register**

FF - Not used for this function

**Data Direction Registers**

1 = Output, 0=input

Reset = 00h

DDR1 – 9F

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| I/O Reg | U7 | U6 | U5 | U4 | U3 | U2 | U1 | U0 |
| Port | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
| Value | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| Pin | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| GTI Func | WDG | P16 | P15 | P14 | P13 | n/c | n/c | IGN |

DDR2 – F0

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| I/O Reg | U15 | U14 | U13 | U12 | U11 | U10 | U9 | U8 |
| Port | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |
| Value | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Pin | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 |
| GTI Func | O/P? | ISC | CEL | INJ | VSS | CAS | IFS | I/P? |

**Swift GTi Timers**

INJ – Fn1, PWC, UDR12, trigger pin UIOR bit0, output pin 36

Injector is triggered by software in the CAS interrupt code, PWC generates a one-shot pulse with compare capability

IGN1 Fn2, CTO, Compare register UDR13, trigger input pin 38 (CAS), trigger enable pin UIOR4 bit4, output pin 46

IGN2 Fn3, OSC, Compare register UDR14, trigger pin 46, output pin 48 (IGN)

Ignition trigger is enabled in software and then a CAS input (which one?) triggers a Combination Trigger One Shot Timer (CTO). The back edge of the one shot pulse generates a trigger signal on pin 46 which triggers a One Shot Timer (OTC) that generates an output pulse that turns on the coil on its leading edge and turns it off on its falling edge.

CAS Fn4, INS, Sample register UDR15, trigger pin 38 (CAS), output pin 48?

ISC – Fn7, PWC, Compare register UDR17, output pin 34, (input pin 36?)

VSS – Fn12, FRC, Counter register UDR9, clock pin 37

VSS is read on a tick generated by TMR1 using a loop counter of 268.

50Hz gives a count of 69 = 1.38seconds = 259\*5.12ms (TMR1)

TMR1 – Fn11, INC, Compare register UDR20, output pin 47 (P11), IRQR bit 1

Function 11 is an interval timer used to provide a system tick. The clock period is 16us (every FE)?,

UDR20 is initialised at 140h/320 giving an interval of 5.12ms

IFS Fn13, FRC, Counter register UDR10, clock pin 39

Free running Counter – counts IFS pulses

TMR2 – Fn6, INC, Compare register UDR16, output pin 44(P14), IRQR bit 4

Initialised to 1900h/6400 giving an interval of 102.4ms

UNKN – Fn8, INC, Compare register UDR18, output pin 43

Initialised to 1388h/5000 giving an interval of 80ms

UNKN – Fn9, PWC, Compare register UDR19, input pin 33, trigger pin 43, output pin 33

UNKN - Fn14, FRC, Counter register UDR11, trigger pin 40

**Function/Pin assignments**

which should tally with the above????

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | U0 | U1 | U2 | U3 | U4 | U5 | U8 | U9 | U10 | U11 | U12 | U14 | U15 |
| UPP Fn | OSC | INC | CTO | INS | INC | INC | FRC | FRC |  | FRC | PWC | PWC | PWC |
| Port | P10 |  | P12 | P13 | P14 | P15 | P20 | P21 | P22 | P23 | P24 | P26 | P27 |
| Pin | 48 |  | 46 | 45 | 44 | 43 | 40 | 39 | 38 | 37 | 36 | 34 | 33 |
| Pin Fn | IGN |  | u/k | u/k | u/k | u/k | u/k | IFS | CAS | VSS | CPV | ISC | u/k |

\*Pulse input pin number 20 corresponds to the UPPIO register UIOR bit 4.

**Interrupts**

IER1 maps to U7-0  
IER2 maps to U15-8  
IER3 maps to U23 -16

IER1 = 6 = pins U2,U1 – u/k  
IER2 = 4 = pin U10 = CAS  
IER3 = 0

ISR1 bit3 used by CAS

IRQR1 – Interrupt Request Register 1

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | IRR7 | IRR6 | IRR5 | IRR4 | IRR3 | IRR2 | IRR1 | IRR0 |
| Port | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
| Pin |  |  |  |  | 45 | 46 | 47 | 48 |
| Pin Fn |  |  |  |  |  | IGN1 CTO | TMR1 | IGN |

IRQR2 – Interrupt Request Register 2

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | IRR7 | IRR6 | IRR5 | IRR4 | IRR3 | IRR2 | IRR1 | IRR0 |
| Port | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |
| Pin |  |  |  |  |  | 38 | 39 |  |
| Pin Fn |  |  |  |  |  | CAS | IFS |  |